Computer System Architecture

Tutorial 3:

1. What general categories of function are specified by computer instruction?

**Processor-memory:** Data may be transferred from processor to memory or from memory to processor.

**Processor-I/O:** Data may be transferred to or from a peripheral device by transferring between the processor and an I/O module.

**Data processing:** The processor may perform some arithmetic or logic operation on data. **Control:** An instruction may specify that the sequence of execution be altered.

1. List and briefly define the possible states that define an instruction execution?

**Instruction address calculation (iac):** Determine the address of the next instruction to be executed.

**Instruction fetch (if):** Read instruction from its memory location into the processor. **Instruction operation decoding (iod):** Analyze instruction to determine type of operation to be performed and operand(s) to be used.

**Operand address calculation (oac):** If the operation involves reference to an operand in memory or available via I/O, then determine the address of the operand.

**Operand fetch (of):** Fetch the operand from memory or read it in from I/O.

**Data operation (do):** Perform the operation indicated in the instruction.

**Operand store (os):** Write the result into memory or out to I/O.

1. List and briefly define two approaches to dealing with multiple interrupts.

(1) Disable all interrupts while an interrupt is being processed. (2) Define priorities for interrupts and to allow an interrupt of higher priority to cause a lower-priority interrupt handler to be interrupted.

1. What is the benefit of using a multiple-bus architecture compared to a single-bus architecture?

**With multiple buses, there are fewer devices per bus. This (1) reduces propagation delay, because each bus can be shorter, and (2) reduces bottleneck effects where slower bus will slow down the whole computer’s performance which has a high speed processor.**

1. What is the different between synchronous and asynchronous bus? What is the advantages of asynchronous bus?

**The occurrence of events on the bus is determined by a clock.**

**The occurrence of one event on a bus follows and depends on the occurrence of a previous event.**

**A mixture of slow and fast devices, using older and newer technology, can share a bus.**

1. Consider a 32-bit microprocessor, with 16-bit external data bus, driven by a 16-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/s?

**Clock cycle time = 1/16 MHz = 62.5 ns**

**Minimum bus cycle time required to transfer 16 bits of data = 4 \* 62.5 = 250 ns**

**In terms of byte, 2 bytes (equals to 16 bits) transfer;**

**Thus, the transfer rate = 2 / 250 ns = 8 Mbytes/s**